Preliminary Amendment
Divisional Application of U.S.S.N. 09/928,126
Attorney Docket No.: ASC-025DV1

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This application is a divisional of application Serial No. 09/928,126, filed on August 10, 2001, which claims priority from provisional application Serial No. 60/225,666, filed August 16, 2000, now expired, the entire disclosures of which are incorporated by reference herein.

## In the Claims:

Please cancel claims 1–53.

Please amend claims 54 and 55 as follows.

54. (Amended) A semiconductor structure comprising:

a substrate including an insulator layer;

a first layer of relaxed  $Si_{1-x}Ge_x$  disposed over the insulator layer, wherein x has a value in the range of 0.1 to 1; and

a second layer disposed over the substrate, the second layer comprising a material selected from the group consisting of GaAs, AlAs, ZnSe, InGaP, and strained Si<sub>1-y</sub>Ge<sub>y</sub> wherein y has a value different from the value of x.

55. (Amended) A semiconductor structure comprising:

a substrate; and

a plurality of layers disposed over the substrate, the layers comprising:

a graded Si<sub>1-x</sub>Ge<sub>x</sub> buffer layer, the graded buffer layer having a Ge concentration x, wherein x has a value that increases from zero to a value y;

a first relaxed layer comprising Si<sub>1-v</sub>Ge<sub>v</sub>; and

a separation layer comprising at least one material selected from the group consisting of strained  $Si_{1-z}Ge_z$  with  $z \neq y$ , III-V materials, and II-VI materials.

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Please add new claims 56-110:

- 56. (New) The structure of claim 54 wherein the value of x is in the range of 0.3 to 1.
- 57. (New) A semiconductor structure comprising:

a substrate;

a first layer of relaxed Si<sub>1-x</sub>Ge<sub>x</sub> disposed over the substrate, x having a value in the range of 0.1 to 1;

a second layer disposed over the substrate, the second layer comprising at least one material selected from the group consisting of GaAs, AlAs, ZnSe, InGaP, and strained Si<sub>1-v</sub>Ge<sub>v</sub> wherein y has a value different from the value of x; and

a plurality of ions disposed in at least one of the first layer and the second layer.

- 58. (New) The structure of claim 57 wherein the ions comprise at least one of hydrogen  $H^+$  ions and  $H_2^+$  ions.
- 59. (New) The structure of claim 55 wherein a surface of the structure has a root mean square surface roughness of less than about 11 angstroms.
- 60. (New) The structure of claim 55, further comprising:

  a second relaxed layer.
- 61. (New) The structure of claim 60 wherein the second relaxed layer comprises relaxed Si<sub>1-w</sub>Ge<sub>w</sub> and w is substantially equal to y.
- 62. (New) The structure of claim 60 wherein y is approximately equal to 1 and the second relaxed layer comprises at least one material selected from the group consisting of Ge, GaAs, AlAs, ZnSe, and InGaP.
- 63. (New) The structure of claim 55, further comprising: a plurality of ions disposed in the structure.

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- 64. (New) The structure of claim 63 wherein the ions comprise at least on of hydrogen  $H^+$  ions and  $H_2^+$  ions.
- 65. (New) The structure of claim 63 wherein the ions are disposed in the separation layer.
- 66. (New) The structure of claim 63 wherein the separation layer comprises a strained layer and the ions are disposed in one of the graded buffer layer and the first relaxed layer.
- 67. (New) The structure of claim 55, further comprising: an oxide layer disposed over the plurality of layers.
- 68. (New) The structure of claim 55, further comprising:

  a device integrated into at least a portion of the plurality of layers.
- 69. (New) The semiconductor structure of claim 55 wherein the separation layer comprises a strained layer.
- 70. (New) The semiconductor structure of claim 55 wherein the separation layer comprises a defect layer.
- 71. (New) A semiconductor structure comprising:

  a substrate comprising silicon;

  an insulating layer disposed over the substrate; and

  a relaxed Si<sub>1-x</sub>Ge<sub>x</sub> layer disposed over the insulating layer, the relaxed Si<sub>1-x</sub>Ge<sub>x</sub>

  layer having a uniform composition and a dislocation defect density of less than 10<sup>6</sup>/cm<sup>2</sup>.
- 72. (New) The structure of claim 71 wherein a Ge concentration x of the relaxed layer is in the range of zero to 1.

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- 73. (New) The structure of claim 72 wherein the Ge concentration x is in the range of 0.3 to 1.
- 74. (New) The structure of claim 71, further comprising:

  a device layer disposed over the relaxed Si<sub>1-x</sub>Ge<sub>x</sub> layer.
- 75. (New) The structure of claim 71 wherein the device layer comprises at least one material selected from the group consisting of strained Si, strained Si<sub>1-y</sub>Ge<sub>y</sub> with  $y \neq x$ , III-V materials, and II-VI materials.
- 76. (New) The structure of claim 71, further comprising:

  a device disposed within at least a portion of the relaxed Si<sub>1-x</sub>Ge<sub>x</sub> layer.
- 77. (New) A semiconductor structure comprising:

  a relaxed Si<sub>1-y</sub>Ge<sub>y</sub> layer disposed on a substrate; and

  a buried layer defined by implanted ions disposed in the relaxed Si<sub>1-y</sub>Ge<sub>y</sub> layer.
- 78. (New) A semiconductor structure comprising:
  a first heterostructure including:
- a graded Si<sub>1-x</sub>Ge<sub>x</sub> buffer layer disposed on a first substrate, the graded Si<sub>1-x</sub>Ge<sub>x</sub> buffer layer having a Ge concentration x increasing from zero to a value y; a relaxed Si<sub>1-y</sub>Ge<sub>y</sub> layer disposed on the graded Si<sub>1-x</sub>Ge<sub>x</sub> buffer layer; and a buried layer defined by implanted ions disposed in one of said graded Si<sub>1-x</sub>Ge<sub>x</sub> buffer layer and relaxed Si<sub>1-y</sub>Ge<sub>y</sub> layer.
- 79. (New) The semiconductor structure of claim 78 wherein the implanted ions comprise at least one of  $H^+$  ions and  $H_2^+$  ions.
- 80. (New) The semiconductor structure of claim 78 wherein a surface of the structure has a roughness less than about 11 nanometers.

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- 81. (New) The semiconductor structure of claim 78, further comprising: an oxide layer disposed over the first heterostructure.
- 82. (New) The semiconductor structure of claim 78 wherein the first heterostructure is bonded to a second substrate, defining a second heterostructure.
- 83. (New) The semiconductor structure of claim 82 wherein the second substrate comprises an insulator layer and the first heterostructure is bonded to the insulator layer.
- 84. (New) The semiconductor structure of claim 83 wherein the insulator layer comprises an oxide layer.
- 85. (New) A semiconductor structure comprising: a substrate; and
- a semiconductor layer bonded to the substrate, the semiconductor layer having a surface roughness of less than about 11.3 nanometers.
- 86. (New) The semiconductor structure of claim 85 wherein the semiconductor layer comprises at least one of relaxed Si<sub>1-y</sub>Ge<sub>y</sub>,GaAs, AlAs, ZnSe, and InGaP.
- 87. (New) The semiconductor structure of claim 86 wherein the semiconductor layer comprises a surface damage layer.
- 88. (New) The semiconductor structure of claim 86 wherein the surface damage layer has a thickness of less than about 100 nanometers.
- 89. (New) The semiconductor structure of claim 85, further comprising: a device disposed within at least a portion of the semiconductor layer.

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90. (New) A semiconductor structure comprising:

a first heterostructure including:

a graded Si<sub>1-x</sub>Ge<sub>x</sub> buffer layer disposed on a first substrate, the graded Si<sub>1-x</sub>Ge<sub>x</sub> buffer layer having a Ge concentration x increasing from zero to 1; a relaxed Ge layer disposed on the graded Si<sub>1-x</sub>Ge<sub>x</sub> buffer layer; a semiconductor layer disposed on the relaxed Ge layer; and a buried layer disposed within at least one of the graded Si<sub>1-x</sub>Ge<sub>x</sub> buffer layer, the semiconductor layer, and the relaxed Ge layer, the buried layer being defined by ions.

- 91. (New) The semiconductor structure of claim 90 wherein the implanted ions comprise at least one of  $H^+$  ions and  $H_2^+$  ions.
- 92. (New) The structure of claim 90 wherein the first heterostructure is bonded to a second substrate, thereby defining a second heterostructure.
- 93. (New) The semiconductor structure of claim 92, further comprising: a device disposed within at least a portion of the semiconductor layer.
- 94. (New) A semiconductor structure comprising:

a first heterostructure including:

a graded  $Si_{1-x}Ge_x$  buffer layer disposed on a first substrate, the graded  $Si_{1-x}Ge_x$  buffer layer having a Ge concentration x increasing from zero to a value y; a relaxed  $Si_{1-z}Ge_z$  layer disposed on the graded  $Si_{1-x}Ge_x$  buffer layer, z being greater than y; and

a buried layer defined by ions disposed within the graded  $\mathrm{Si}_{1\text{-}x}\mathrm{Ge}_x$  buffer layer.

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- 95. (New) The semiconductor structure of claim 94 wherein the implanted ions comprise at least one of  $H^+$  ions and  $H_2^+$  ions.
- 96. (New) The semiconductor structure of claim 94 wherein the first heterostructure is bonded to a second substrate, defining a second heterostructure.
- 97. (New) The semiconductor structure of claim 94, further comprising: a device disposed within at least a portion of the semiconductor layer.
- 98. (New) A semiconductor structure comprising:

  a substrate; and

  a relaxed Si<sub>1-z</sub>Ge<sub>z</sub> layer bonded to the substrate,

  wherein a surface of the Si<sub>1-z</sub>Ge<sub>z</sub> layer is defined by a selective etch.
- 99. (New) A semiconductor structure comprising: a first heterostructure including:
- a graded Si<sub>1-x</sub>Ge<sub>x</sub> buffer layer disposed on a first substrate, wherein the graded Si<sub>1-x</sub>Ge<sub>x</sub> buffer layer has a Ge concentration x increasing from zero to a value y; a relaxed Si<sub>1-y</sub>Ge<sub>y</sub> layer disposed on the graded Si<sub>1-x</sub>Ge<sub>x</sub> buffer layer; a separation layer disposed on the relaxed Si<sub>1-y</sub>Ge<sub>y</sub> layer; a second relaxed layer disposed over the separation layer; and a plurality of ions disposed in at least one of the graded buffer layer, the relaxed layer, the separation layer, and the second relaxed layer.
- 100. (New) The semiconductor structure of claim 99 wherein the implanted ions comprise at least one of  $H^+$  ions and  $H_2^+$  ions.
- 101. (New) The semiconductor structure of claim 99 wherein the first heterostructure is bonded to a second substrate, defining a second heterostructure.

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- 102. (New) The semiconductor structure of claim 101, further comprising:

  a device disposed within at least a portion of the second heterostructure.
- 103. (New) A semiconductor structure comprising:a relaxed layer bonded to a substrate; anda strained layer disposed on the relaxed layer.
- 104. (New) The structure of claim 103 wherein the relaxed layer comprises a material selected from the group consisting of relaxed Si<sub>1-w</sub>Ge<sub>w</sub>, Ge, GaAs, AlAs, ZnSe, and InGaP.
- 105. (New) The structure of claim 103 wherein the strained layer comprises a material selected from the group consisting of strained Si<sub>1-z</sub>Ge<sub>z</sub> and III-V material.
- 106. (New) The semiconductor structure of claim 103, further comprising: a device disposed within at least a portion of the strained layer.
- 107. (New) A semiconductor structure comprising: a first heterostructure including:
  - a layer structure comprising:

a graded  $Si_{1-x}Ge_x$  buffer layer disposed on a first substrate, wherein the Ge concentration x increases from zero to a value y, and

a relaxed  $Si_{1-z}Ge_z$  layer disposed over the graded  $Si_{1-x}Ge_x$  buffer layer, wherein z is substantially equal to or greater than y; and a buried layer disposed in the layer structure.

108. (New) The structure of claim 107 wherein the buried layer comprises implanted ions.

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- 109. (New) The structure of claim 107 wherein the implanted ions comprise at least one of hydrogen  $H^+$  ions and  $H_2^+$  ions.
- 110. (New) The structure of claim 107, wherein the first heterostructure is bonded to a second substrate to define a second heterostructure.